	Type	Hits	Search Text
1	BRS	36	redundan$2 adj select$4 adj line$1
2	BRS	91	shift$4 adj redundan$2
3	BRS	1427507	fault$4 or error$4 or problem$
4	BRS	415	decod$4 adj signal$4 adj line$1
5	BRS	0	two-bit adj shift$4 adj redundan$2
6	BRS	0	one-bit adj shift$4 adj redundan$2
7	BRS	2	(redundan$2 adj select$4 adj line$1) same (shift$4 adj redundan$2)
8	BRS	0	((redundan$2 adj select$4 adj line$1) same (shift$4 adj redundan$2)) same (fault$4 or error$4 or problem$)
9	BRS	0	((redundan$2 adj select$4 adj line$1) same (fault$4 or error$4 or problem$)) same (decod$4 adj signal$4 adj line$1)
10	BRS	79318	switch$4 adj (circuit$ or operation$)
11	BRS	0	((redundan$2 adj select$4 adj line$1) same (fault$4 or error$4 or problem$)) same (switch$4 adj (circuit$ or operation$))
12	BRS	35166	memory adj cell$
13	BRS	2	((redundan$2 adj select$4 adj line$1) same (fault$4 or error$4 or problem$)) and (switch$4 adj (circuit$ or operation$))
14	BRS	10	(redundan$2 adj select$4 adj line$1) same (fault$4 or error$4 or problem$)
15	BRS	221	plural$4 adj select$4 adj line$1
16	BRS	248	(redundan$2 adj select$4 adj line$1) or (plural$4 adj select$4 adj line$1)
17	BRS	0	((redundan$2 adj select$4 adj line$1) or (plural$4 adj select$4 adj line$1)) same (fault$4 or error$4 or problem$) same (decod$4 adj signal$4 adj line$1)
18	BRS	1	((redundan$2 adj select$4 adj line$1) or (plural$4 adj select$4 adj line$1)) and (fault$4 or error$4 or problem$) and (decod$4 adj signal$4 adj line$1)

	DBs	Time Stamp	Comments	Error Definition
1	USPAT; US-PGPUB	2002/01/17 12:22		
2	USPAT; US-PGPUB	2002/01/17 12:22		
3	USPAT; US-PGPUB	2002/01/17 12:22		
4	USPAT; US-PGPUB	2002/01/17 12:23		
5	USPAT; US-PGPUB	2002/01/17 12:23		
6	USPAT; US-PGPUB	2002/01/17 12:23		
7	USPAT; US-PGPUB	2002/01/17 10:52		
8	USPAT; US-PGPUB	2002/01/17 10:53		
9	USPAT; US-PGPUB	2002/01/17 10:54		
10	USPAT; US-PGPUB	2002/01/17 12:29		Truncation overflow.
11	USPAT; US-PGPUB	2002/01/17 10:58		
12	USPAT; US-PGPUB	2002/01/17 11:00		Truncation overflow.
13	USPAT; US-PGPUB	2002/01/17 11:00		
14	USPAT; US-PGPUB	2002/01/17 12:04		
15	USPAT; US-PGPUB	2002/01/17 12:30		
16	USPAT; US-PGPUB	2002/01/17 12:07		
17	USPAT; US-PGPUB	2002/01/17 12:08		
18	USPAT; US-PGPUB	2002/01/17 12:17		

	Type	Hits	Search Text
19	BRS	2487	(714/?).ccls.
20	BRS	1721	(711/?).ccls.
21	BRS	575	(365/?).ccls.
22	BRS	4728	((714/?).ccls.) or ((711/?).ccls.) or ((365/?).ccls.)
23	BRS	0	(((redundan$2 adj select$4 adj line$1) or (plural$4 adj select$4 adj line$1)) and (((714/?).ccls.) or ((711/?).ccls.) or ((365/?).ccls.))) and (decod$4 adj signal$4 adj line$1)
24	BRS	4	((redundan$2 adj select$4 adj line$1) or (plural$4 adj select$4 adj line$1)) and (((714/?).ccls.) or ((711/?).ccls.) or ((365/?).ccls.))
25	BRS	20	redundan$2 adj select$4 adj line$1
26	BRS	117	shift$4 adj redundan$2
27	BRS	2169201	fault$4 or error$4 or problem$
28	BRS	61	decod$4 adj signal$4 adj line$1
29	BRS	0	two-bit adj shift$4 adj redundan$2
30	BRS	0	one-bit adj shift$4 adj redundan$2
31	BRS	97831	switch$4 adj (circuit$ or operation$)
32	BRS	41	plural$4 adj select$4 adj line$1
33	BRS	56	(redundan$2 adj select$4 adj line$1) or (plural$4 adj select$4 adj line$1)
34	BRS	80	((redundan$2 adj select$4 adj line$1) or (plural$4 adj select$4 adj line$1)) or (shift$4 adj redundan$2)

	DBs	Time Stamp	Comments	Error Definition
19	USPAT; US-PGPUB	2002/01/17 12:17		
20	USPAT; US-PGPUB	2002/01/17 12:18		
21	USPAT; US-PGPUB	2002/01/17 12:18		
22	USPAT; US-PGPUB	2002/01/17 12:18		
23	USPAT; US-PGPUB	2002/01/17 12:19		
24	USPAT; US-PGPUB	2002/01/17 12:19		
25	EPO; JPO; DERWENT; IBM_TDB	2002/01/17 12:22		
26	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/01/17 12:22		
27	EPO; JPO; DERWENT; IBM_TDB	2002/01/17 12:23		
28	EPO; JPO; DERWENT; IBM_TDB	2002/01/17 12:23		
29	EPO; JPO; DERWENT; IBM_TDB	2002/01/17 12:23		
30	EPO; JPO; DERWENT; IBM_TDB	2002/01/17 12:23		
31	EPO; JPO; DERWENT; IBM_TDB	2002/01/17 12:30		
32	EPO; JPO; DERWENT; IBM_TDB	2002/01/17 12:30		
33	EPO; JPO; DERWENT; IBM_TDB	2002/01/17 12:31		
34	EPO; JPO; DERWENT; IBM_TDB	2002/01/17 12:31		

	Type	Hits	Search Text
35	BRS	13	(((redundan$2 adj select$4 adj line$1) or (plural$4 adj select$4 adj line$1)) or (shift$4 adj redundan$2)) and (fault$4 or error$4 or problem$)

	DBs	Time Stamp	Comments	Error Definition
35	EPO; JPO; DERWENT; IBM_TDB	2002/01/17 12:31		

gates 206 and 208. Both sets of NAND gates 202, 204 and 206, 208 receive the
YSG signal on one of their other inputs. Referring to FIG. 10, the YSG latches
200 have their outputs RCTL and CTL of complementary polarity. Thus, the NAND
gates 202, 204 and 206, 208 are responsible for switching the YSG signal to
either RYSG.sub.-- B or YSG.sub.-- B.

DOCUMENT-IDENTIFIER: US 5959903 A
TITLE: Column redundancy in semiconductor memories

---------- KWIC ---------

ABPL:
This invention describes a column redundancy method and apparatus in a DRAM that minimizes the timing difference between a normal and redundant column paths and which minimizes the number of fuses required in repairing **faulty** columns. The invention discloses a DRAM having memory elements arranged in rows and columns, the memory elements being accessible by decoding a memory address applied thereto, normal column drivers for energizing appropriate memory columns in response to the decoder memory addresses received at an input thereof; redundant column drivers; and switch means for steering the decoded memory address onto one of either normal or redundant column driver paths. The invention further illustrates a fusing system which minimizes the capacitance of **redundant select lines,** thereby removing unnecessary delay in the redundant column path.

DEPR:
Each column driver has associated therewith address decoder and **switching circuitry** as indicated by block 30. For the sake of simplicity the circuit configuration for a redundancy scheme according to the present invention will be described with reference to the single circuit block 30 associated with normal driver Y0, however this circuit block 30 is duplicated for each of drivers Y1 to Y63 respectively. Thus referring to the circuit shown in block 30, pre-decoded address signals PY.sub.i,j, PY.sub.k,l, PY.sub.m,n,p indicated by numeral 33 are applied to the inputs of a NAND gate 34. The output 35 of the NAND gate is coupled to an input 40 of normal driver Y0, via a switch formed by first and second NMOS transistors 36 and 38, respectively. The first NMOS transistor 36 has its source-drain circuit connected between the output

node 35 of the NAND gate 34 and the input 40 of normal driver Y0. The second
NMOS transistor 38 has its source-drain circuit connected between the output
node 35 of the NAND gate 34 and an input node 42 of redundant driver R0. The
input node 42 of redundant driver R0 is held high by a fuse 43 connected
between a VDD supply and the input node 42. The gate 36g of the first
transistor 36 and the gate 38g of the second transistor 38 are each connected
to complementary signals REN and REN, respectively. The REN signal is derived
from the output of a Vpp powered inverter 46, which has connected to its input
the signal REN. A fuse 48 is connected at one end thereof to the input of the
inverter 46. The other end of the fuse is connected to an NMOS transistor 44,
which has its source-drain circuit connected between a ground node 47 the fuse
48. When enabled, transistor 44 maintains REN "low" if no redundancy is
required. First and second PMOS transistors 54 and 56 respectively have their
respective source-drain circuits connected between the VPP voltage supply and
the input node of the invester 46. The VPP supply is an internally generated
boosted voltage supply derived from a VDD level supply voltage. The gate of
the first PMOS transistor 54 is connected to the gate of the NMOS transistor 44
that in turn is connected to a reset input RST. The RST input signal is
derived from an external source (not shown). The gate of the second PMOS
transistor 56 is connected to the gate of the first NMOS transistor 36. A
pass-gate formed by a PMOS transistor has its source-drain circuit connected
between the VDD supply and the source output of the first NMOS transistor 36.
The gate of the pass-gate PMOS transistor is also connected to the gate of the
first NMOS transistor 36.

DEPR:
Referring now to FIG. 4, a schematic diagram of a normal Y driver is shown
generally by numeral 60. A block indicated by numeral 62 is a detailed
implementation of a normal Y driver indicated as blocks Y0 to Y63 in FIG. 3.
Such an implementation is already known in the art and, therefore, will not be
discussed further. Other suitable driver circuit implementations may be

equally well be used for block 62. The decoding-**switching circuitry** is as
shown in FIG. 3. Furthermore, standard decoding or pre-decoding techniques can
be used to generate the inputs 33 in FIG. 3.

DEPR:
Referring to FIG. 6 an architectural implementation consisting of sixty-four
normal column decoders and two redundant column decoders is shown generally by
numeral 60. The normal column drivers Y0 to Y63 and their associated decoders
and **switching circuitry** 31 correspond to those shown in FIG. 3. The fuse 48
shown in FIG. 3 is indicated schematically in FIG. 6 by numeral 64. As also
described earlier with reference to FIG. 3, pre-decoded address signals
PY.sub.i,j, PY.sub.k.l, PY.sub.m.n.p are applied to the decoders 31. The
driver/decoders are arranged in two blocks B0 and B1, each block comprised of
drivers Y0 to Y31 and Y32 to Y63 respectively arranged on either side of a pair
of redundant column drivers R0 and R1. The redundant driver R0 may be
connected to replace the columns addressed by odd numbered drivers Y1, Y3 . .
. Y63 along a line RYSEL.sub.-- 0. While the redundant driver R1 may be
connected to replace the columns addressed by even numbered drivers Y0, Y2 . .
. Y62 along a line RYSEL.sub.-- 1. The fuses 43 for maintaining the
RYSEL.sub.-- 0 and RYSEL.sub.-- 1 lines high are indicated by numeral 66. In
addition to these fuses, each of the redundant driver R0 and R1 include a fuse
RYSEL0.sub.-- L, RYSEL0.sub.13 R and RYSEL1.sub.-- L, RYSEL1.sub.-- R
respectively connected on either side of their respective input nodes 68 and 70
and inline with their respective RYSEL lines; these fuses correspond to fuses
70 and 72 in FIG. 5.

DOCUMENT-IDENTIFIER: US 6137735 A
TITLE: Column redundancy circuit with reduced signal path delay

---------- KWIC ---------

BSPR:
In FIG. 3, a redundancy circuitry 10 is implemented which uses an address steering approach according to an embodiment of the invention in U.S. patent application Ser. No. 08/904,153 to Chen et al. assigned to MOSAID Technologies Inc. In this approach, each Y decoder consists of an NMOS multiplexer 12 which steers the column select signal either down the normal or redundant paths according to the information programmed in the fuse circuit 14. NMOS transistors are used in conjunction with an on-chip boosted voltage supply VPP to select the appropriate path since the NMOS transistors in the multiplexer require a voltage larger than VDD to fully turn them on. The **redundant select line** RYSEL 16 is long and exhibits considerable RC delay. In this implementation two redundant column drivers are accessible by 64 normal columns, but the redundant drivers are dedicated to replacing **faulty** columns only in that block and can not be used to replace **faulty** columns in any other blocks within a quadrant. This lack of flexibility proves to be intolerable when moving from the 64M SDRAM density to the 256M SDRAM density. Furthermore, the length of the RYSEL line 16 makes such a design too slow for the 256M generation SDRAM.

DEPR:
Referring to FIG. 9, the YSG **switching circuit** 72 (FIG. 4) is shown in detail. The **switching circuit** includes a pair of YSG latches 200 coupled to latch and delay the input RDEC signal. The YSG signal is held for two clock cycles due to the dual data bus architecture. The output RYSG.sub.-- B(1:0) and YSG.sub.-- B(1:0) are coupled to the redundant driver 70 and the normal Y drivers respectively. The RCTL (redundant decoder control) output from the latches 200 are coupled to an input of respective gates 202 and 204, while a CTL (decoder control) output is coupled to the inputs of a second pair of NAND

The
resistance element R should have such a resistance value as enabling the
potential on the corresponding local word line LWL (2j) or LWL (2j+1) to attain
a sufficiently high level when the potential on the corresponding main word
line /MWLL or /MWLR and the potential on the corresponding Z **decoder signal
line** ZL are at a low level and a high level, respectively, in spite of
discharging through the resistance element R. For example, the resistor R may
have a resistance value as large as 10 k.OMEGA. in consideration of the
current drivability of transistor 24a.

DEPR:
In the embodiment shown in FIG. 15, in order to reliably force each of the
local word lines LWL (2j) and LWL (2j+1) to 0 V when both of the corresponding
complementary main word line pair of /MWLL and MWLL or MWLR and MWLR, and the
corresponding Z **decoder signal line** ZL are not activated, a resistance element
R is provided as a discharging path from the local word line to ground GND.
However, the discharging path is not necessarily formed by a resistance element
but may be formed by any element having the same function as a resistance
element. For example, as shown in FIG. 16, N channel MOS transistor 24f having
a gate connected to power supply Vcc may be used for this discharging path.
Transistor 24f should have approximately the same ON resistance value as that
of resistance element 15 of FIG. 15.

DEPR:
FIG. 18 is a circuit diagram showing one example of an arrangement of the
respective local decoders LD (2j) and LD (2j+1) of FIG. 17. FIG. 18 shows, as
a representative, two adjacent local decoders LD (2j) and LD (2j+1) connected
to the same Z **decoder signal line** /ZL of FIG. 17.

DEPR:
With reference to FIG. 18, the arrangement of the respective local decoders LD
(2j) and LD (2j+1) of the present embodiment is obtained by interchanging the
even-numbered main word line /MWLL and the odd-numbered main word line /MWLR
with the Z **decoder signal line** ZL in the local decoders shown in FIG.

13.

DEPR:
More specifically, in each local decoder LD (2j) provided corresponding to each even-numbered block BL (2j) of the present embodiment, the gates of transistors 24a and 24b are connected to the corresponding Z **decoder signal line** /ZL and the sources of transistors 24a and 24c are connected to the corresponding even-numbered main word line MWLL. Similarly, in each local decoder LD (2j+1) provided corresponding to each odd-numbered block BL (2j+1), the gates of transistors 24a and 24b are connected to the corresponding Z **decoder signal line** /ZL and the sources of transistors 24a and 24c are connected to the corresponding odd-numbered main word line MWLR.

DEPR:
In the present embodiment, the signal line connected to the gates of transistors 24a and 24b and the signal line connected to the sources of transistors 24a and 24c are signal lines a low level potential on which is regarded as being in an inactive state and a signal line a high level potential on which is regarded as being in an active state, respectively. Therefore, similarly to the local decoder arranged as shown in FIG. 13, each of the local decoders LD (2j) and LD (2j+1) of the present embodiment activates the corresponding local word line LWL (2j) or LWL (2j+1) only when the corresponding complementary main word line pair of /MWLL and MWLL or /MWLR and MWLR, and the corresponding Z **decoder signal line** /ZL are both activated.

DEPR:
With reference to FIG. 19, unlike the embodiment shown in FIG. 11, one even-numbered main word line MWLL and one odd-numbered main word line MWLR are provided corresponding to each of the sub-block groups SBL0-SBL127 in the present embodiment. Therefore, each local decoder LD (2j) is connected only to the corresponding even-numbered main word line MWLL and the corresponding Z **decoder signal line** /ZL. Similarly, each local decoder LD (2j+1) is connected only to the corresponding odd-numbered main word line MWLR and Z **decoder signal line** /ZL.

DEPR:

FIG. 20 is a circuit diagram showing an arrangement of the local decoders
LD0-LD31 of FIG. 19. FIG. 20 shows two adjacent local decoders LD (2j) and LD
(2j+1) connected to one Z **decoder signal line** /ZL as a representative.

DEPR:
In the local decoders (2j) and LD (2j+1) shown in FIG. 20, the main word lines
MWLR and MWLL are interchangeable with the Z **decoder signal line** /ZL. In this
case, in order that each of the local decoders LD (2j) and LD (2j+1) activates
the corresponding local word line LWL (2j) or LWL (2j+1) only when both of the
corresponding main word line MWLL or MWLR and the corresponding Z **decoder**
signal line /ZL are activated, a signal line connected to the gates of
transistors 24a and 24b and a signal line connected to the source of transistor
24a should be a signal line a low level potential on which is regarded as being
in an active state and a signal line a high level potential on which is
regarded as being in an active state, respectively.

DEPR:
FIG. 21 is a circuit diagram showing a still further example of an arrangement
of the main part of the SRAM of FIG. 1 according to still further embodiment of
the present invention, wherein a main word line and a Z **decoder signal**
line in
each local decoder arranged in the embodiment shown in FIG. 20 are interchanged
with each other.

DEPR:
FIG. 22 is a circuit diagram showing one example of an arrangement of the local
decoders LD0-LD31 of FIG. 21. FIG. 22 shows two adjacent local decoders LD
(2j) and LD (2j+1) connected to one Z **decoder signal line** ZL of FIG. 21 as a
representative.

DEPR:
Therefore, as shown in FIG. 25, a change of an external address signal (FIG.
25(a)) is followed by the output (FIG. 25(b)) of ATD circuit 17 attaining a
high level for a fixed time period and consequently, the potential on the Z
decoder signal line /ZL (FIG. 25(c)) of FIG. 20 once attains a high level
without fail in response to the change of the external address signal. As a

DOCUMENT-IDENTIFIER: US 4849939 A
TITLE: Semiconductor memorizing device

---------- KWIC ---------

CLPV:
a memory array having a plurality of memory cells and a **plurality of selecting lines** coupled to said memory cells, respectively;

CCXR:
714/7

CLIPPEDIMAGE= JP02001006389A
PAT-NO: JP02001006389A
DOCUMENT-IDENTIFIER: JP 2001006389 A
TITLE: SEMICONDUCTOR MEMORY

PUBN-DATE: January 12, 2001

INVENTOR-INFORMATION:

NAME	COUNTRY
ETO, SATOSHI	N/A
MATSUMIYA, MASATO	N/A
KIKUTAKE, AKIRA	N/A

ASSIGNEE-INFORMATION:

NAME	COUNTRY
FUJITSU LTD	N/A

APPL-NO: JP11171303
APPL-DATE: June 17, 1999

INT-CL (IPC): G11C029/00; G06F012/16 ; G06F013/16 ; G11C011/413 ; G11C011/401
; G11C016/06

ABSTRACT:
PROBLEM TO BE SOLVED: To improve a yield of semiconductor chip production by relieving three or more defect selection lines occurring in a semiconductor chip when the device is provided with a redundancy shifting function by using **redundancy selection lines** when defects occur in a part of **plural selection lines**.

SOLUTION: This semiconductor memory comprises two or more 1st **redundancy selection lines** JL0, JL1 located at the end of **plural selection lines**, two or more 2nd **redundancy selection lines** located at the other end, and two steps of a 1st and a 2nd switch parts 2-1, 2-2 connecting **decoding signal lines** to be changed over to the selection lines or the **redundancy selection lines**. Here, when defective selection lines occur, a 1st changeover is operated to shift one or more **decoding signal lines** in the direction of the 1st **redundancy selection lines** JL0, JL1 by a 1st switching part 2-1, or a 2nd changeover is

operated to
shift them in the direction of the 2nd **redundancy selection line** JR0, JR1, or a
3rd changeover is operated to shift one or more **decoding signal lines** in the
direction of the 1st **redundancy selection lines** JL0, JL1 by a 2nd switching
part 2-2, or a 4th changeover is operated to shift them in the direction of the
2nd **redundancy selection line** JR0, JR1.

DOCUMENT-IDENTIFIER: US 6134176 A
TITLE: Disabling a defective element in an integrated circuit device having
redundant elements

---------- KWIC ---------

DEPR:
A technical advantage of the present invention includes providing flip-flops 20
for disabling respective normal word lines 12. Generally, with flip-flops 20,
defective normal elements can be effectively disabled without encountering the
problems associated with previously developed techniques for disabling
defective elements. Specifically, these flip-flops 20 and associated circuitry
(e.g., NAND gates 50, inverters 48, inverters 52, first and second power up
initialization signals 46 and 28, and **redundant select line** 45) are relatively
small. With flip-flops 20, fuses are not needed to "de-program" any defective
normal word lines 12. In addition, flip-flops 20 and the associated circuitry
do not require a significant amount of wiring for support. Accordingly, the
present invention can be implemented in a relatively small chip area and avoids
complex wiring schemes. Furthermore, disabling of a defective normal word line
12 with a corresponding flip-flop 20 avoids the "race" **problem** characteristic
of some prior art techniques.

DOCUMENT-IDENTIFIER: US 5457655 A
TITLE: Column redundance circuit configuration for a memory

---------- KWIC ---------

DEPR:
A small quadrature-access current component flows during the period T2 from the high potential VDD through the transistors P1 and P2, and in the worst case through half of all of the n-channel transistors with non-separated fuse elements, toward the low potential VSS. However this current, which appears when the memory in all of the circuits CF.sub.i,j are completely **error**-free, can be kept extremely slight by means of the dimensioning of the transistors P1 and P2 and by means of a minimum time period T2. This above all exploits the circumstance that for DRAM memories, a relatively long period of time is available for block decoding of the column redundance. The input part of the circuit CF.sub.i,j which is responsible for this block decoding, therefore need not have an especially high speed. In the event that all of the circuits CF.sub.i,j of one unit E.sub.j are inactive, all of the transistors N3 block.
Due to the turned-on p-channel transistor PE1 (ATDN="0"), the line RDN.sub.j is then logical "1", and consequently the output line RDC.sub.j and the **redundant selection line** RCSL.sub.j are logical "0". If, as is explained below, the control signal ATDN rises to high potential, the state of logical "1" of the line RDN.sub.j is maintained by the turned-on retention transistors PE2 with the gate at logical "0". If all of the lines RD.sub.j have the state of logical "0", as is assumed in the first part of FIG. 7, then all of the **redundant selection lines** RCSL.sub.1 . . . 4 are inactive at logical "0", and all four n-channel transistors ND.sub.1 . . . 4 of the gate DNOR are blocked.
The node D, even with the control signal ATDN in the state of logical "1", remains logical "1" because of the turned-on p-channel retention transistor PD2.

DOCUMENT-IDENTIFIER: US 5270975 A
TITLE: Memory device having a non-uniform redundancy decoder arrangement

---------- KWIC ---------

DEPR:
From the above discussion it is clear that one method of maximizing repair
efficiency with a given number of **redundant select lines** in each data block is
to assign multiple decoders to each of the select lines so that each line is
capable of replacing up to a predetermined number of defective column portions
with segments taken from a single redundant column. Thus, when presented with
the **problem** of maximizing production yield, one approach would be to place as
many redundant column select lines on a chip as permitted by the space
constraints; and, uniformly distributing the decoders among the redundant lines
so that each line is capable of repairing the same number of defects.

DOCUMENT-IDENTIFIER: US 4538245 A
TITLE: Enabling circuit for redundant word lines in a semiconductor memory
array

---------- KWIC ---------

DEPR:
Memory 2 is additionally provided with a redundant array 32 of storage devices
4 arranged along redundant word lines 34 for the purpose of providing back-up
storage capacity should any of the primary word lines 10 in primary array 6
prove **faulty**, i.e., should any of the storage devices 4 associated with primary
word lines 10 contain manufacturing defects. The redundant word lines 34 are
connected to the control gates 14 of storage devices 4 to establish alternate
x-addresses for the memory. When a **faulty** word line is present at a particular
x-address in primary array 6, address indicators AI.sub.5 -AI.sub.12 and
inverted address indicators AI.sub.5 -AI.sub.12 generated by address buffers 18
as a function of the address bits A.sub.5 -A.sub.12 corresponding to the
x-address of the **faulty** primary word line are used to program a redundancy
decoder 36 such that any subsequent address signal A.sub.0 -A.sub.12 having the
x-address of the **faulty** word line in primary array 6 will instead enable a
selected redundant word line 34 in redundant array 32. A series of control
signals supplied to **redundancy select lines** 37 via the output pads 28
associated with data bits O.sub.0 -O.sub.3 are gated through a set of
redundancy enable transistors 38 to assist in programming redundancy decoder
36. Once a particular x-address has been transferred from primary array 6 to
redundant array 32, a redundancy disable circuit 39 prevents any accidental
reprogramming of redundancy decoder 36 relative to the selected redundant word
line 34 enabled by the particular x-address. The redundancy disable circuit
additionally generates a redundancy disable signal RD.sub.1 -RD.sub.4
indicative of the fact that the selected redundant word line is in use, which
redundancy disable signal can be supplied back through redundancy enable

DOCUMENT-IDENTIFIER: US 4535259 A
TITLE: Sense amplifier for use with a semiconductor memory array

---------- KWIC ---------

DEPR:
Memory 2 is additionally provided with a redundant array 32 of storage devices
4 arranged along redundant word lines 34 for the purpose of providing back-up
memory capacity should any of the primary word lines 10 in primary array 6
prove **faulty**, i.e., should any of the storage devices 4 associated with primary
word lines 10 contain manufacturing defects. The redundant word lines 34 are
connected to the control gates 14 of storage devices 4 to establish alternate
x-addresses for the memory. When a **faulty** word line is present at a particular
x-address in primary array 6, address indicators AI.sub.5 -AI.sub.12 and
inverted address indicators AI.sub.5 -AI.sub.12 generated by address buffers 18
as a function of the address bits A.sub.5 -A.sub.12 corresponding to the
x-address of the **faulty** primary word line are used to program a redundancy
decoder 36 such that any subsequent address signal A.sub.0 -A.sub.12 having the
x-address of the **faulty** word line in primary array 6 will instead enable a
selected redundant word line 34 in redundant array 32. A series of control
signals supplied to **redundancy select lines** 37 via the output pads 28
associated with data bits O.sub.0 -O.sub.3 are gated through a set of
redundancy enable transistors 38 to assist in programming redundancy decoder
36. Once a particular x-address has been transferred from primary array 6 to
redundant array 32, a redundancy disable circuit 39 prevents any accidental
reprogramming of redundancy decoder 36 relative to the selected redundant word
line 34 enabled by the particular x-address. The redundancy disable circuit
also generates a redundancy disable signal RD.sub.1 -RD.sub.4 indicative of the
fact that the selected redundant word line is in use, which redundancy disable
signal can be supplied back through redundancy enable transistors 38 to an
appropriate output pad 28. A more detailed explanation of the

structure and
function of redundant array 32, redundancy decoder 36 and redundancy disable
circuit 39 can be found in co-pending application Ser. No. 367,331 filed Apr.
12, 1982, and incorporated herein by reference.

DOCUMENT-IDENTIFIER: US 5282175 A
TITLE: Semiconductor memory device of divided word line

---------- KWIC ---------

ABPL:
In a SRAM of a selected word line structure, each local decoder is connected to
a corresponding main word line and a corresponding Z **decoder signal line**. Each
local decoder includes a circuit including two MOS transistors connected in
series to each other which circuit has one end grounded. The corresponding
local word line is connected to a node between these two transistors. Out of
the corresponding main word line and the corresponding Z **decoder signal line**,
one is connected to the gates of these transistors and the other is connected
to the other end of said circuit, which the other end is not grounded. The
potential on the corresponding local word line attains a high level only when
the potential on the signal line connected to the gate of these two
transistors, is at a logical level at which the transistor can be turned on and
the potential on said one signal line is at a high level. Theoretically,
therefore, each local word line is controlled to be activated or inactivated by
the operations of two elements in the corresponding local decoder.

BSPR:
While such **problem** can be avoided to a certain degree by increasing a size of
transistors in address signal decoding circuit to increase a drivability of
address signal decoding circuit 106 with respect to the word line WL, it is not
possible to increase a size of elements in a semiconductor integrated circuit
device without limit. Therefore, the word line WL should be driven by the
elements of a limited size provided in address signal decoding circuit 106
irrespective of an increase of the word line length. The **problem** cannot be
resolved in this manner.

BSPR:
As a conventional technique for avoiding such **problem** as described above, each